AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A method for VLSI chip design comprising the steps of:

estimating signal routes between functional blocks;

determining resistance and capacitance values for the estimated signal routes; and

building a model of said signal routes including resistance and capacitance values;

wherein the VLSI chip design is in register transfer language.

2. (Original) A method according to claim 1 further comprising the step of: foliating nodes in estimated signal routes.

3. (Original) A method according to claim 1 further comprising the step of: generating a connectivity net list from said model.

4. (Original) A method according to claim 1 wherein said step of estimating is performed based on input of a floor plan and a connectivity description.

5. (Original) A method according to claim 4 wherein said step of estimating is performed in response to one or more control factor inputs.

6. (Original) A method according to claim 5 wherein said control factor input specifies a signal routing algorithm.

7. (Original) A method according to claim 4 wherein said step of estimating is performed based on input of signal route configuration parameters.

8. (Original) A method according to claim 7 wherein said signal route configuration parameters specify one or more of signal route material, physical size of signal route material or spacing.

9. (Original) A method according to claim 7 wherein said step of estimating is performed in response to one or more control factor inputs.

10. (Original) A method according to claim 9 wherein said control factor input specifies a signal routing algorithm.

11. (Previously Presented) A VLSI chip whose design was performed according to a method comprising the steps of:

estimating signal routes between functional blocks;

determining resistance and capacitance values for the estimated signal routes; and

building a model of said signal routes including resistance and capacitance values;

wherein the design is in register transfer language.

12. (Original) A VLSI chip according to claim 11 whose design was performed according to the method further comprising the step of:

foliating nodes in estimated signal routes.

13. (Original) A VLSI chip according to claim 11 whose design was performed according to the method further comprising the step of:

generating a connectivity net list from said model.

14. (Original) A VLSI chip according to claim 11 whose design was performed according to the method wherein said step of estimating is performed based on input of a floor plan and a connectivity description.

15. (Original) A VLSI chip according to claim 14 whose design was performed according to the method wherein said step of estimating is performed in response to one or more control factor inputs.

16. (Original) A VLSI chip according to claim 15 whose design was performed according to the method wherein said control factor input specifies a signal routing algorithm.

17. (Original) A VLSI chip according to claim 14 whose design was performed according to the method wherein said step of estimating is performed based on input of signal route configuration parameters.

18. (Original) A VLSI chip according to claim 17 whose design was performed according to the method wherein said signal route configuration parameters specify one or more of signal route material, physical size of signal route material or spacing.

19. (Original) A VLSI chip according to claim 17 whose design was performed according to the method wherein said step of estimating is performed in response to one or more control factor inputs.

20. (Original) A VLSI chip according to claim 19 whose design was performed according to the method wherein said control factor input specifies a signal routing algorithm.

21. (Previously Presented) A system for forming a VLSI chip design comprising:

means for estimating signal routes between functional blocks;

means for determining resistance and capacitance values for the estimated signal routes; and

means for building a model of said signal routes including resistance and capacitance values;

wherein the VLSI chip design is in register transfer language.

22. (Previously Presented) A method according to claim 1 wherein the estimating signal routes between functional blocks occurs prior to a layout for the VLSI chip design.

23. (Previously Presented) A VLSI chip according to claim 11 wherein the estimating signal routes between functional blocks occurs prior to a layout for the VLSI chip.

24. (Previously Presented) A system according to claim 21 wherein the estimating signal routes between functional blocks occurs prior to a layout for the VLSI chip design.

25. (New) The method of claim 1 wherein determining comprises:

determining resistance values and capacitance values for the estimated signal routes.

26. (New) The method of claim 11 wherein determining comprises:

determining resistance values and capacitance values for the estimated signal routes.

27. (New) The system of claim 21 wherein the means for determining comprises:

means for determining resistance values and capacitance values for the estimated signal routes.